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EXAMINER	
ALROBAYE, IDRISS N	

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2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/796,499	ESPOSITO, BEN	
	Examiner	Art Unit	
	Idriss N. Alrobaye	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 April 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This action is responsive to communications through the applicant's application filed on 12/03/2007.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peng U.S. Patent No. 5,594,675 (hereinafter Peng) in view of Ema et al. U.S. Patent No. 2002/0130944 (hereinafter Ema).

4. As per claim 1, Peng teaches digital signal processing (DSP) circuitry that independently processes a plurality of multi-channel data signals, comprising:

a plurality of columns of registers (see e.g. Fig. 11, elements 734-0, 734-1, 734-u-1 etc), each said column comprising a single input (see e.g. Fig. 11, wherein each column has a single input starting with the first register in each column) and a plurality of registers arranged in serial as a sequence of registers (see e.g. Fig. 11, element 734-1, wherein column 734-1 has plurality of registers and are arranged in series as a sequence of registers) wherein the single input is coupled to a register of the plurality of

registers that is positioned first in the sequence of registers (see Fig. 11, element 734-1, wherein the single input of element 734-1 is coupled to a register 'REG L' of the plurality of registers 'REG L to REG 1' that is positioned first in the sequence of registers (REG L is positioned first in the sequence)); and

interconnection circuitry for allowing successive channels of said plurality of multi-channel data signals to be selectively shifted through said plurality of registers in each said column (see e.g. Fig. 11, element 734-1, and col. 17, lines 5-23) and to also be selectively shifted through a plurality of registers in at least one other of said plurality of columns (see e.g. Fig, 11, element 734-0 "one column", element 734-1 "another column", wherein one input of MUX1 (element 732-1) comes from column 734-0), wherein said interconnection circuitry allows a value at the single input of each column to be selectively routed to any said register in said respective column (see e.g. Fig. 11, wherein the a value at the single input of each column is selectively routed to any said register. For instance, column 734-1 can route values from the single input to any of the registers, REG L, REG L-1, REG 1. If column 734-1 wants to route values from the column input to REG L-1, the values will pass through REG L until it reaches REG L-1. Similarly with REG 1, if the values from column 734-1 to be routed to REG 1, the values will have to go through REG L and REG L-1, but eventually will reach REG 1).

Although Peng did not explicitly show bypassing any register or registers that precede said register in said respective column. However, this implementation is well known in the art, it's a very similar structure to a shift register. One of ordinary skill in the art would recognize this implementation as an obvious matter of design choice.

Nevertheless, since the reference Peng did not show "bypassing any register or register...", the examiner introduces a secondary reference (Ema) that explicitly show the last limitation. Ema teaches bypassing any register or registers that precede said register in said respective column (see Ema, Fig. 14, wherein the load values 'i.e., Load1, Load2, etc' bypasses any register or registers that precede said register in said respective column), for the purpose of easily passing and manipulating data to any register in the column.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Ema in the invention of Peng, for the purpose of easily manipulating data within registers and allowing fast and parallel shifting of data within registers because the connection 'Load' is directly connected to each register. Furthermore, simultaneous updating registers thus significantly improving performances.

5. As per claim 2, Peng further teaches the circuitry of claim 1, further comprising utilization circuitry for operating on a first piece of data output by a register in a first of said columns and a second piece of data output by a register in a second of said columns (see e.g. Fig. 11), wherein the first and second pieces of data each corresponds to a first channel of the plurality of multi-channel data signals (see e.g. Fig. 11, and Fig. 5).

6. As per claim 3, Peng further teaches the circuitry of claim 2, wherein said utilization circuitry comprises circuitry selected from the group consisting of adder circuitries, multiplier circuitries, and a combination thereof (see e.g. Fig. 11, elements 740-0, 740-1, multiplier).

7. As per claim 4, Peng further teaches the circuitry of claim 1, wherein the interconnection circuitry comprises:

a multiplexer circuit associated with each register in each said column (see Peng, e.g. Fig. 5, wherein a multiplexer is associated with each register in each column; see column that contains element 413-1, 412-0-1, 412-0-L; register 412-0-1 is associated with MUX 413-1 and 412-0-L is associated with MUX in i=2).

8. As per claim 5, Peng further teaches the circuitry of claim 1, wherein said interconnection circuitry allows successive data signals to be shifted to as many different said plurality of columns as needed such that the output of each of those columns is used as an input to a finite impulse response filter function (see e.g. Fig. 11; abstract; col. 1, lines 1-67; col. 6, lines 65-67; col. 16, lines 5-20).

9. As per claim 6, Peng further teaches the circuitry of claim 5, wherein a respective register in each of those columns provides a respective piece of the output data used as the input to the filter function (see e.g. Fig. 11, abstract; col. 1, lines 1-67; col. 6, lines 65-67; col. 16, lines 5-20), wherein each respective piece of the output data

corresponds to a first channel of the plurality of multi-channel data signals (see e.g. Fig. 5).

10. As per claim 7, Peng further teaches the circuitry of claim 1, wherein said interconnection circuitry can selectively route data signals past one or more of said registers in each said column (see e.g. Fig. 11, wherein the output of column 734-1, REG 1 is going to the input of MUX1 (element 732-1)).

11. As per claim 8, Peng further the circuitry of claim 1 wherein said circuitry is mounted on a programmable logic device (The digital signals processing as taught by Peng is considered equivalent to a programmable logic device).

12. As per claim 9, Peng further teaches the programmable logic device defined in claim 8 further comprising:

routing circuitry for selectively supplying signals to and receiving signals from the DSP circuitry (see e.g. Figs. 10-11).

13. As per claim 10, Peng further teaches the programmable logic device defined in claim 9 further comprising:

programmable logic circuitry connected to the routing circuitry (see e.g. Fig. 4, wherein element 310 is connected to element 340 (which contain the routing circuitry)).

14. As per claim 11, Peng further teaches a digital processing system comprising:

processing circuitry (see e.g. Fig. 4);

a memory coupled to the processing circuitry (see e.g. Fig. 4, elements 310 and 320); and

a programmable logic device as defined in claim 8 coupled to the processing circuitry and the memory (see e.g. Fig. 4, element 340).

15. As per claim 12, Peng further teaches the circuitry of claim 8 wherein said circuitry is mounted on a printed circuit board (it's understood from Peng reference that the DSP is mounted on a printed circuit board).

16. As per claim 13, Peng further teaches the printed circuit board defined in claim 12 further comprising:

a memory (see e.g. Fig. 4, element 320 and 310) mounted on the printed circuit board and coupled to the programmable logic device (see e.g. Fig. 4, element 340; It's understood from Peng reference that the circuit is mounted on a printed circuit board).

17. As per claim 14, Peng further teaches the printed circuit board defined in claim 12 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the programmable logic device (see e.g. Fig. 4, wherein elements 330 and 350 are processing circuitry and are connected to the control logic 340).

18. As per claim 15, it's rejected for the same reasons set forth above in claim 1, wherein the columns in claim 1 are considered equivalent to the tap delay line circuitry in claim 15.

19. As per claims 16-21, claims 1-14 have all the features that claims 16-21 have, thus claims 16-21 are rejected for the same reasons set forth above in claims 1-14. The only different is naming, wherein the tap delay line circuitry in claims 16-21 is considered equivalent to the columns of registers in claims 1-14.

20. As per claim 22, Ema further teaches the circuitry of claim 1, wherein the interconnection circuitry comprises:

a first multiplexer circuit associated with a first register in a first of said columns (Ema, Fig. 14, element 131, first mux; the mux that is connected to P13; the mux is associated with the first register); and

a second multiplexer circuit associated with a second register in the first column (Ema, Fig. 14, element 131, second mux; the mux that is connected to P9);

wherein each of the first and second multiplexer circuits is operative to select between a same first value (Ema, Fig. 14, wherein 'LOAD 1' is equivalent to a same first value) and a different second value (Ema, Fig. 14, wherein P13 and P9 are different values) for application to the respective first and second registers (Fig. 14, first and second registers of element 131), wherein the same first value is the value at the input

of the first column (Fig. 14, LOAD 1) and the different second value is an output from a register that precedes the first and second registers respectively in the first column (Fig. 14, wherein the output from a register that precedes the first and second register respectively in the first column). The motivation utilized in the combination of claim 1, super, applies equally as well to claim 22.

21. As per claim 23, Ema further teaches the circuitry of claim 22, wherein the first and second multiplexer circuits each comprises a respective first and a respective second input (Ema, Fig. 14, element 131 first and second multiplexer), wherein:

the respective first inputs of the first and second multiplexer circuits are coupled to each other and to the input of the first column (Ema, Fig. 14, element 131, first and second multiplexer); and

the register that precedes the second register in the first column is the first register wherein the second input of the second multiplexer is coupled to the output of the first register (Ema, Fig. 14, element 131, first and second registers). The motivation utilized in the combination of claim 1, super, applies equally as well to claim 23.

22. As per claims 24-25, they are rejected for the same reasons set forth above in claims 22-23.

23. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Washakowski et al. U.S. Patent Application Publication No. 2005/0238117 (hereinafter Washakowski) in view of Ema.

24. As per claim 15, Washakowski teaches a programmable logic device (PLD), comprising:

digital signal processing (DSP) circuitry that supports multiple channels of data being transmitted on the same carrier, said DSP circuitry (see e.g. Fig. 1, wherein I and Q are the channels) comprising:

tap delay line circuitry (see e.g. Fig. 2A-2D, wherein element 200I and 200Q are the tap delay line circuitry; see paragraphs [0023]-[0024]) that comprises registers (see e.g. Fig. 4C, channels I and Q) for registering the data of each of the multiple channels such that the data of each channel is not mixed with the data of any other channel (see e.g. Fig. 2A-2D; and Fig. 4C, where it two shows the two separate channels I and Q, elements 440I and 440Q), wherein the registers are arranged in serial as a sequence of registers (see Fig. 4C and Fig. 2A-2D) wherein the tap delay line circuitry comprises:

a single input coupled to a register of the plurality of registers that is positioned first in the sequence of registers (see Fig. 2A-2D and Fig. 4C wherein each tap delay line circuitry has a single input that is positioned first in the sequence of registers); and

interconnection circuitry that allows a value received at the single input to e selectively routed to any of said registers in said tap delay line circuitry (see e.g. Fig 4C, wherein the value received at the input of the channel can be routed to any registers.

The value may passes through other registers in order to route the value into the selected register)

utilization circuitry that performs a function on data received from said tap delay line circuitry (see e.g. Fig. 2A-2D, wherein the adder, element 206I and 206Q are the utilization circuitry).

Although Washakowski did not explicitly show bypassing any register or registers that precede said register in said tap delay line circuitry. However, this implementation is well known in the art, it's a very similar structure to a shift register. One of ordinary skill in the art would recognize this implementation as an obvious matter of design choice.

Nevertheless, since the reference Washakowski did not show "bypassing any register or register...", the examiner introduces a secondary reference (Ema) that explicitly show the last limitation. Ema teaches bypassing any register or registers that precede said register in said line circuitry (see Ema, Fig. 14, wherein the load values 'i.e., Load1, Load2, etc' bypasses any register or registers that precede said register in said line circuitry), for the purpose of easily passing and manipulating data to any register in the column.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Ema in the invention of Washakowski, for the purpose of easily manipulating data within registers and allowing fast and parallel shifting of data within registers because the connection 'Load' is

directly connected to each register. Furthermore, simultaneous updating registers thus significantly improving performances.

25. Claims 16-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Washakowski in view Ema and further in view of Peng.

26. As per claim 16, Washakowski further teaches the PLD of claim 15, wherein said tap delay line circuitry comprises:

at least two columns of registers, each column including at least two registers arranged in serial (see Washakowski, Fig. 4C);

Washakowski did not specifically teach the structure as described below (a multiplexer circuit respectively associated with a register of each said column, said multiplexer....).

Peng teaches the structure as described here: a multiplexer circuit respectively associated with a register of each said column (see Peng, Fig. 11, multiplexers (732-0 to 732-u); columns (elements 735-0 to 735-u); registers in each column (734-0 to 735-u), said multiplexer circuit operative to select one of at least two input signals being applied to said multiplexer circuit for application to said associated register (Fig. 11, column 735-0), one of said input signals being one of said plurality of multi-channel signals, and another one of said input signals being the output signal of a register that is conveyed by a tap delay line from a register in a column different than the column said multiplexer circuit applies said input signal to (Fig. 11, columns, elements 735-0 and

735-1). Peng teaches the structure as described above for the purpose of reducing processing requirements (Peng, col. 19, lines 61-67).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Peng in the invention of Washakowski, for the purpose of improving FIR filters by merging cross-symmetric bank filter terms. The merging of the filter banks enables a dramatic reduction in processing time and circuit size requirements without impeding the performance of the filter (Peng. col. 6, lines 40-44;col. 19, lines 61-67).

27. As per claim 17, Washakowski in view of Peng teaches the invention as claimed above. Peng further teaches the DSP circuitry of claim 16, wherein said associated register is a leading register in each said column (see Peng, Fig. 11, columns 735-0 to 735-u and REG L in each column). The motivation utilized in the combination of claim 16, super, applies equally as well to claim 17.

28. As per claim 18, Washakowski in view of Peng teaches the invention as claimed above. Peng further teaches the DSP circuitry of claim 16, wherein the output signal of the register being conveyed by the tap delay line is the output of a trailing register in each said column (see Peng, Fig. 11, columns 735-0 to 735-u and REG 1 in each column). The motivation utilized in the combination of claim 16, super, applies equally as well to claim 18.

29. As per claim 19, Washakowski in view of Peng teaches the invention as claimed above. Peng further teaches the DSP circuitry of claim 16, wherein the tap delay line conveys an output signal of a register that is being provided to a first tap to a multiplexer circuit associated with a column that provides an output signal to a second tap (see Peng, Fig. 11, columns 735-0 to 735-1). The motivation utilized in the combination of claim 16, super, applies equally as well to claim 19.

30. As per claim 20, Washakowski in view of Peng teaches the invention as claimed above. Peng further teaches the DSP circuitry of claim 15, wherein said utilization circuitry selectively operates on signals output by a register in each said column. (See Peng, e.g. Fig. 11, multipliers 740-0 to 740-u). The motivation utilized in the combination of claim 16, super, applies equally as well to claim 20.

31. As per claim 21, Washakowski in view of Peng teaches the invention as claimed above. Peng further teaches the DSP circuitry of claim 16, further comprising bypass circuitry for enabling the selected input signal to be routed directly to one of said at least two registers in said column of registers (see Peng, e.g. Fig. 11, column 735-0, wherein the output of REG 1 is feedback to the MUX1 and to REG L). The motivation utilized in the combination of claim 16, super, applies equally as well to claim 21.

32. As per claim 22, Ema further teaches the circuitry of claim 1, wherein the interconnection circuitry comprises:

a first multiplexer circuit associated with a first register in a first of said columns (Ema, Fig. 14, element 131, first mux; the mux that is connected to P13; the mux is associated with the first register); and

a second multiplexer circuit associated with a second register in the first column (Ema, Fig. 14, element 131, second mux; the mux that is connected to P9);

wherein each of the first and second multiplexer circuits is operative to select between a same first value (Ema, Fig. 14, wherein 'LOAD 1' is equivalent to a same first value) and a different second value (Ema, Fig. 14, wherein P13 and P9 are different values) for application to the respective first and second registers (Fig. 14, first and second registers of element 131), wherein the same first value is the value at the input of the first column (Fig. 14, LOAD 1) and the different second value is an output from a register that precedes the first and second registers respectively in the first column (Fig. 14, wherein the output from a register that precedes the first and second register respectively in the first column). The motivation utilized in the combination of claim 15, super, applies equally as well to claim 22.

33. As per claim 23, Ema further teaches the circuitry of claim 22, wherein the first and second multiplexer circuits each comprises a respective first and a respective second input (Ema, Fig. 14, element 131 first and second multiplexer), wherein:

the respective first inputs of the first and second multiplexer circuits are coupled to each other and to the input of the first column (Ema, Fig. 14, element 131, first and second multiplexer); and

the register that precedes the second register in the first column is the first register wherein the second input of the second multiplexer is coupled to the output of the first register (Ema, Fig. 14, element 131, first and second registers). The motivation utilized in the combination of claim 15, super, applies equally as well to claim 23.

34. As per claims 24-25, they are rejected for the same reasons set forth above in claims 22-23.

Response to Arguments

35. Applicant's arguments filed 12/03/2007 have been fully considered but they are not persuasive.

36. **Applicant's Argument**:

"First, applicant respectfully submits that shift register structures do not function to have a value from an input coupled to a register positioned first in a sequence of registers bypass another register in the sequence, as defined by applicant's claims 1 and 15. Instead, shift register structures operate to either shift data in-line when activated or to load parallel data into each of the registers. When data is shifted in-line, the data is moved sequentially from one register to the next and none of the data bypasses any register in the column of registers. In the latter case, for data to be loaded in parallel, multiple inputs, corresponding to different portions of the parallel data are required for loading the value present at each input into a corresponding register of the register column. Thus, it is not the value of the single input coupled to the first register in the sequence of registers that bypasses another register in the sequence or column, but the value at an input coupled to a register positioned later in the sequence that arguably bypasses a previous register in the column. Accordingly, even if one skilled in the art were to modify the Peng device with shift registers (as suggested by the Examiner), one skilled in the art would not arrive at applicant's claimed invention. Therefore, Peng and

the suggested modification using shift registers as an obvious matter of design choice does not show or suggest all the features of applicant's claimed invention."

Examiner's Response

The examiner respectfully disagrees. Looking at applicant's drawing Fig. 2, registers and muxes structure and comparing that with Ema Fig. 14 registers and muxes structure. One of ordinary skill in the art at the time of the invention was made would recognize that the structure of the registers and muxes shown in Fig. 14 of Ema are the same structure of the registers and muxes of applicant's drawing Fig. 2. Also, one of ordinary skill in the art at the time the invention was made would recognize that the registers and muxes shown in Fig. 14 of Ema are able to perform the same functionalities as the registers and muxes shown in applicant's drawing Fig. 2

37. **Applicant's Argument**:

"Second, applicant respectfully submits that Ema does not show or suggest having a value from an input coupled to a register positioned first in a sequence of registers bypass another register in the sequence, as defined by applicant's claims 1 and 15. Instead, Ema shows shift registers 131 that have multiple inputs, each associated with a different register in the series of registers 131, required to enable the loading of parallel data (i.e., PI-PI3). In Ema, when the load signal is asserted, it is the portion (e.g., P9) of the parallel data (e.g., PI3, P9, P5 and PI) that is received by a register positioned later in the sequence (e.g., positioned second in the sequence) that bypasses the other registers in the shift registers 131 and not the value at the single input coupled to the first register in the sequence (e.g., PI3). Moreover, the value at the first register in the sequence has to pass through every subsequent register in the sequence to reach a register positioned later in the sequence and thus the value does not bypass any of the subsequent registers in the column. Thus, contrary to the Examiner's assertions, Ema does not make up for the deficiencies of Peng relative to the rejection. Therefore, Peng and Ema, whether taken alone, or in combination, do not show or suggest all the features of applicant's claims."

Examiner's Response:

The examiner respectfully disagrees. Looking at applicant's drawing Fig. 2, registers and muxes structure and comparing that with Ema Fig. 14 registers and muxes structure. One of ordinary skill in the art at the time of the invention was made would recognize that the structure of the registers and muxes shown in Fig. 14 of Ema are the same structure of the registers and muxes of applicant's drawing Fig. 2. Also, one of ordinary skill in the art at the time the invention was made would recognize that the registers and muxes shown in Fig. 14 of Ema are able to perform the same functionalities as the registers and muxes shown in applicant's drawing Fig 2.

Furthermore, as shown in Fig. 14 of Ema, the registers have a single input going into the 'D' input of the registers. Element 131 of Fig. 14 of Ema, first register is positioned first in a sequence of registers.

Also, Peng teaches a plurality of columns of registers (see e.g. Fig. 11, elements 734-0, 734-1, 734-u-1 etc), each said column comprising a single input (see e.g. Fig. 11, wherein each column has a single input starting with the first register in each column) and a plurality of registers arranged in serial as a sequence of registers (see e.g. Fig. 11, element 734-1, wherein column 734-1 has plurality of registers and are arranged in series as a sequence of registers) wherein the single input is coupled to a register of the plurality of registers that is positioned first in the sequence of registers (see Fig. 11, element 734-1, wherein the single input of element 734-1 is coupled to a register 'REG L' of the plurality of registers 'REG L to REG 1' that is positioned first in the sequence of registers (REG L is positioned first in the sequence));

38. **Applicant's Argument**:

"The Examiner rejected claim 15 as being obvious from Washakowski in view of Ema (Office Action, page 8). But, in the same rejection, the Examiner stated that "Peng did not explicitly show bypassing" and "since the reference Peng did not show bypassing.., the examiner introduces [EMA]" (Office Action, page 9, ¶¶ 5 and 6, emphasis added). Applicant understands this to mean that Washakowski does not show or suggest bypassing any register or registers that precede said register in said tap delay line circuitry since Peng was not relied upon in the rejection."

Examiner's Response:

The examiner agrees with the applicant's assertion. The rejection has been corrected to recited Washakowski instead of Peng.

Conclusion

39. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

40. The following is text cited from 37 CFR 1.111U.S. Patent No.: In amending reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

41. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- U.S. Patent No. 5,144,525 shows analog acquisition system including a high-speed timing generator.
- U.S. Patent No. 6,421,251 shows an array board interconnect system
- U.S. Patent Application Publication No. 2002/0130944 shows a light-emission modulation having effective scheme of creating Gray scale on image
- U.S. Patent Application Publication No. 2002/0089348 shows programmable logic integrated circuit devices including dedicated processor components.
- See also attached PTO-892 form.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Idriss N. Alrobaye whose telephone number is 571-270-1023. The examiner can normally be reached on Mon-Fri from 8:00 to 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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